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# System Level Behavioral Modeling of CORDIC Based ORA of Built-in-Self-Test for Sigma-Delta Analog-to-Digital Converter

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***Abstract*** - This paper gives a novel approach CORDIC technique and test generation for the testing of mixed signal circuits component such as analog-to-digital converter. The sigma delta modulator's static parameters such as gain and offset error and nonlinearity errors as well as dynamic parameter i.e. the degradation of signal-to-noise ratio(SNR) value are directly obtained by the Simsides (a MATLAB SIMULINK tool). Then, the obtained parameters are tested by using Built-in-self-test. BIST is desirable for the VLSI system in order to reduce the cost per chip of production –time testing by the manufacture, it can also provide the means to perform in-the field diagnostic. Therefore, this paper will demonstrate a possibility to simplify modeling and simulation of testing strategy of high-resolution sigma delta modulator using MATLAB SIMULINK environment. Here, we are concentrating towards the Output Response Analyzer (ORA) of the BIST. The appropriate approximation of testing parameters reduces the difficulties in designing the complete ORA circuit. In addition, the reusable features of hardware in the computation of different parameters further improve the ORA design. A sigma delta modulation based signal generator is considered which can produce analog sinusoidal test stimuli and digital reference signal on chip. By comparing the ADC output with that of the generator reference signal, the parameter can be determined on chip based on the standard equations in the proposed simulation environment.

***Keywords*****:** *On-Chip Signal Generator; Output Response Analyzer; CORDIC.*

## I. INTRODUCTION

With the increase in functionality of integrated on a single chip is basically a digital-driven trend. In order, to communicate with the outside or say analog world, analog-to-digital (A/D) and digital-to-analog (D/A) converter plays an important role towards the interfacing between analog and digital domains [3-5]. Analog-to-digital Converter (ADC) is widely used as a mixed signal device in many of the system-on-chip designs. Now a day, a trend toward integrating the complete mixed signal system onto a single chip is in heights. So with reduced size, cost and power consumption, the promotion towards the development of new generation of electronics system accomplishing all major features for the interaction of real time world to the digital processing circuitry is in its great demand.

The task of testing a VLSI chip to guarantee its functionality is exceptionally complex and often very time taking. In addition to the difficulty of testing the chips (IC) themselves, the incorporation of the chips into systems has caused test generation's cost to grow highly. The broadly recognized methodology to deal with the testing

problem at the chip level is to incorporate built-in self-test (BIST) capability inside a chip. This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier [5-7]. In conventional testing, test patterns are produced externally through the help of computer aided design tools(CAD). The test patterns and the expected responses of the circuit under test to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. On the other hand, in built-in self-test, the test pattern generation and the output response evaluation are done on chip; thus, the use of high-end automatic test equipment (ATE) machines to test chips can be avoided.[10-12].

High-resolution ADCs with high sampling rates are required in a broad area of high-performance applications, such as high-grade imaging systems,wireless communications, and radar[14-18]. To deliver ADCs satisfying the requirements of the applications, it is obligatory that they are tested as less time as possible, but without negotiating the quality of the test. The analog to digital converter is the standard of the mixed circuit and this circuit is the most exclusive to test due both to the ADCs standard tests being quite long and to the high price of mixed signal testers and other test instruments[19-22]. The use of BIST techniques relieves the dependency on costly test equipment and allows delivering low-cost devices [23-27].

### *A. Sigma-Delta converters*

Sigma delta converters work at oversampling. That means the sampling frequency is much greater than message signal (Fm). Compared with Nyquist rate ADCs, oversampling ADCs gets high resolution in spite of analog components it uses digital signal processing for performing analog-to-digital conversion and due to the oversampling sigma-delta ADCs; they do not need steep roll-off anti-alias filtering, which is the prime requirement of Nyquist rate ADCs. Thus, higher order with better and higher linearity is no used and generally avoided to clarify why the study was undertaken and what hypotheses were tested.

## II. METHODS

### *A. On-chip signal generator*

The subsystem of Built-in Self-Test generates test stimulus signal which is a sinusoidal signal. The generated signal is trustful and highly configurable and also easily adjustable frequencies. A digital resonator based on a Lossless Discrete Integrator (LDI) biquad circuit is used as test stimulus generator. The resonator can be formed by cascading two discrete-time integrators.

For on-chip test stimulus generation, a digital resonator based on a Lossless Discrete Integrator (LDI) biquad circuit [2] is used. The resonators are formed by cascading two discrete-time integrators of the form z-1/ (1-z-1) and 1/ (1- z-1) in a loop with the sign of one integrator being positive and the other negative. This arrangement is shown in Figure 1.

Two facts are important for the digital resonator. The first one is that variations in the coefficients a21and a12may cause shifts in the oscillation frequency. Assuming the resonator is clocked at a rate fos= 1/T, the oscillation frequency w0 will take the following form:

$$w_0 = f_{os} cos^{-1}\left(1 - \frac{a_{12}a_{21}}{2}\right) \quad for \quad 0 < a_{12}a_{21} \leq 4 \tag{1}$$

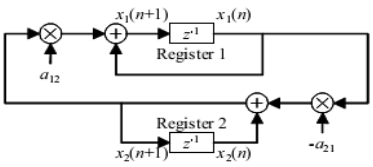



**Figure 1.** *Test Stimulus Generator.*

The second fact is that the amplitude (A) and phase (∅) of the oscillating tone depend on the initial conditions imposed on registers x1and x2. Precisely, it will be;

$$A = \frac{(1-a_{12}a_{21})x_1(0)+a_{12}x_2(0)}{\sin(w_0T+\emptyset)} \quad (2)$$

$$\emptyset = tan^{-1}\left(\frac{x_1(0)\sin(w_0T)}{(1-a_{12}a_{21}-\cos(w_0T))x_1(0)+a_{12}x_2(0)}\right) \quad (3)$$

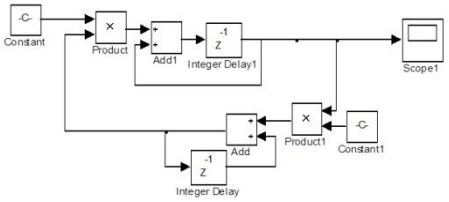



**Figure 2.** *( II ) Simulink Model of Test Stimulus Generator.*

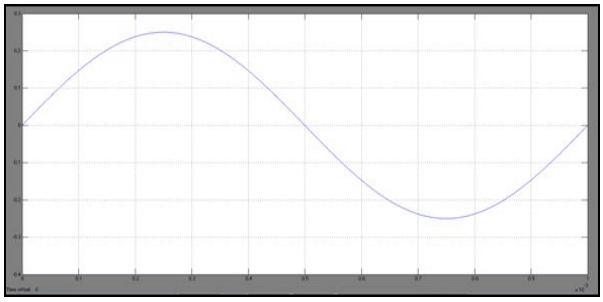


**Figure 4.:** *Scope Output of Stimulus Generator ($a_{21}=2^{-6}$, $a_{12}= 2.677\times10^{-4}$,$x_1(0) = 0$ and $x_2(0) = 0.0327249$, $f_{os}= 3.072$MHz.*

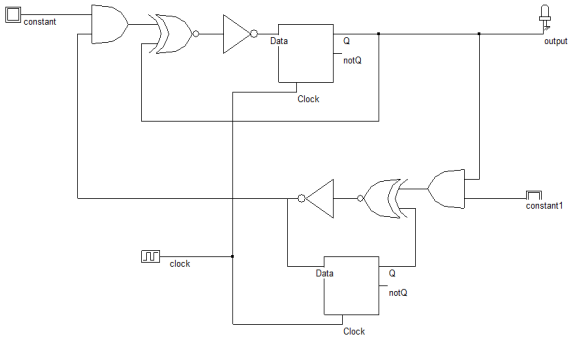



**Figure 3.***:( III ) Approximate Gate Level RealizationTest Stimulus Generator.*

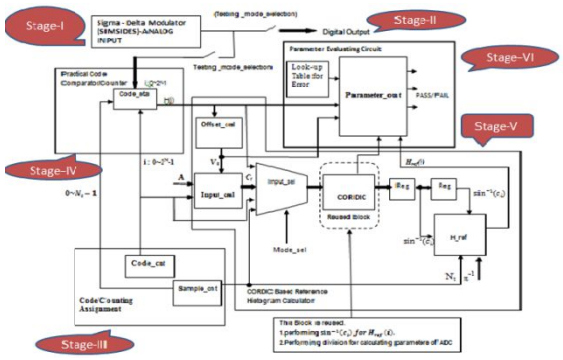



**Figure 5.***CORDIC based ORA*

**Stage-I:** This stage consists of the On-chip signal generator as well as the design of Sigma-Delta ADC using SIMSIDES. This very first stage gives its output to the Stage-II and Stage IV.

**Stage-II:** This stage simply represents the digital output obtained from Stage-I.

**Stage-III:** Third stage is the stage of Code/Counting Assignment consists of two counters:-

- Code_cnt
- Sample_cnt.

**Stage-IV:** It consists of Code_sta which compares the output from stage-I to the output from stage-II and accordingly the counter will increment its value. So, called as Practical code Comparator/Counter

**Stage-V:** This block makes all the necessary calculations required by the response analyzer and hence termed as CORDIC-based Reference Histogram Calculator.

**Stage-VI:** Parameter evaluating circuit gives the overall output of the Response Analyzer in the form of Pass/Fail. The divided block diagram with reference to figure 5.

### *B. ADC under test (Stage-I)*

The circuit under test (CUT) is a second order sigma delta modulator designed by using SIMSIDES. SIMSIDES (SIMULINK-based Sigma-Delta Simulator) is a MATLAB SIMULINK tool having S-function blocks using switched capacitor technique.

1) **For giving the input:** In this experiment we have taken sine wave generator as the input.
2) **For generating the SIMSIDES output:** After applying input to the sigma delta modulator its output is given for testing
3) **For getting the BIST output:** The SIMSIDES output is given to the ORA of the BIST Circuit and the testing parameters are obtained.

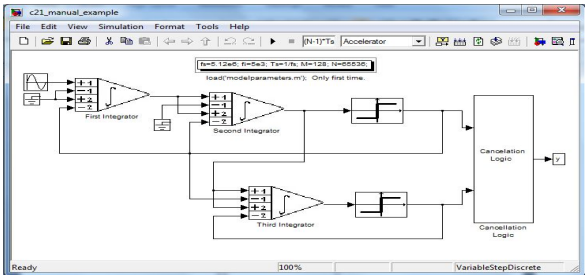
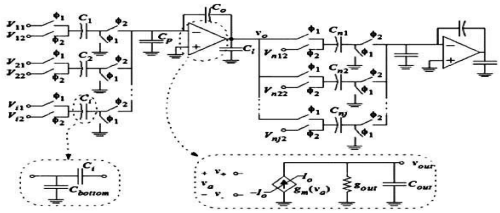



**Figure 6.** *SIMULINK SIMSIDES model for second order Sigma-Delta Modulator*

The op-amp based switched capacitor circuit for the second order Sigma-Delta Modulator is given as:



### *C. Output Response Analyzer*

The ORA of the BIST system has been designed by using Coordinate Rotation Digital Computer (CORDIC) technique. This technique is applied to establish the sine wave reference histogram on chip with sufficient accuracy.

The CORDIC technique gives an iterative formulation to evaluate many elementary functions, like logarithm, trigonometric function and division, using a shift-and-add approach.

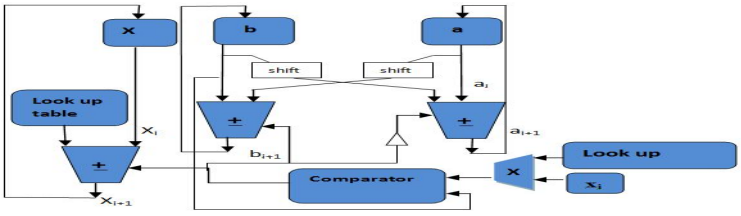



**Figure 8.** *Block diagram of basic CORDIC technique [12]*

## III. RESULTS AND DISCUSSION

### *A. Calculation of INL and DNL*

Based on the theoretical calculation of INL and DNL shown in figure 6 the output from the CORDIC Technique can be calculated, but the practical calculation will be made directly from the SIMSIDES. The practical calculation is shown in figs 4 and 5 where, first graph give the characteristic of DNL while the second graph shows the characteristic of INL.

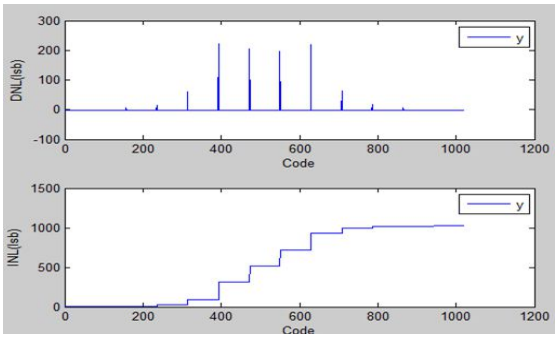



**Figure 9.**: *Output Response of the INL and DNL*

### *B. Output Response of CORDIC*

After the designing of CORDIC for the self testing a comparative graph between the reference and the CORDIC will be obtained and hence shown in fig 9. This figure is the output of stage 6 as per the fig 10.

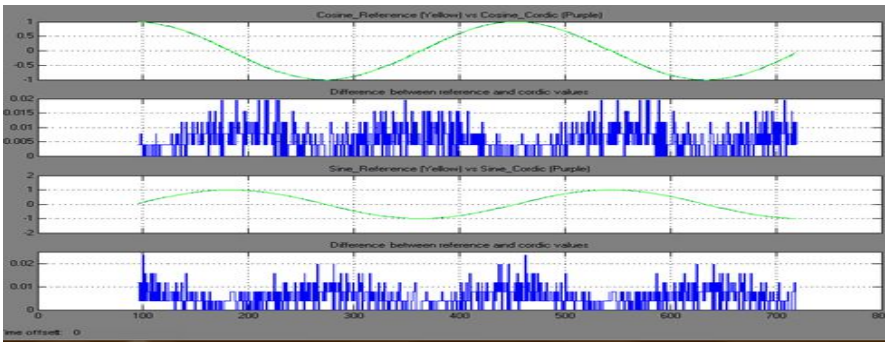



**Figure 10.***Comparison between output of SIMSIDES and CORDIC*

*a- Comparison with Previous Work*

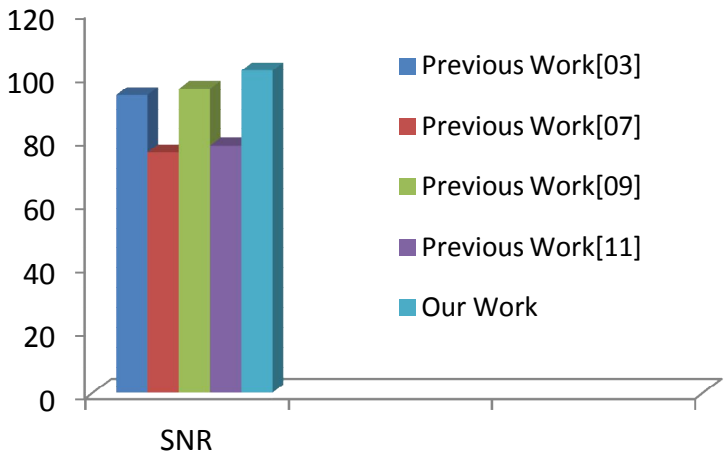



**Figure 11.** *Comparison with Previous Work*

*b- Table*

**Table 1.** *Comparing the Modulators parameters of our work with previous work*

| **Simulated Specifications** | | |
|---|---|---|
| **Specification** | **Values** | |
| DNL | ± 0.234 LSB | |
| INL | ± 0.2431 LSB | |
| SNR | 101.7833 | |
| **Estimated Specifications** | | |
| **Specification** | **Previous Work** | **Our Work** |
| □DNL | ≤ ± 0.01 LSB | ≤ ± 0.01 LSB |
| □INL | ≤ ± 0.01 LSB | ≤ ± 0.01 LSB |
| SNR | -0.860 | -0.92 |
| Data-bit width | 13 bit | 13 bit |

## IV. CONCLUSION AND FUTURE SCOPE

With the help of digital resonator based on a Lossless Discrete Integrator (LDI) biquad circuit, we can reduce the area of the stimulus generator and also we can easily change the test stimulus frequency. Through 2nd Order low pass Sigma Delta analog to digital converter, we can improve the resolution and signal to noise ratio as well as we can reduce the power consumption and increase the ENOB. We have to take care of the Non Idealities like clock jitter, op-amp noise etc. so that it will not affect the performance of the circuit. A behavioral model of built-in self-test with 2nd order low-pass sigma-delta modulator including the non-idealities (sampling jitter, thermal noise, op-amp noise, slew rate and bandwidth) design under test are studied. The special design could be applied to overcome the non-idealities. A GUI-based implementation has been made to calculate the dynamic specification (SNR and ENOB) of sigma delta analog to digital converter. In this thesis, we found that by implementing this technique is area efficient with better performance. The value of SNR and ENOB are found to be 109.9 dB and 17.97 bits respectively in comparison to the 86.7, 94.7 dB & 14.11, 15.44 bits respectively of the previous work. Since the value of SNR and ENOB are increased it makes the respective signal power and resolution better. In this paper, a structure of the ORA circuit for the second order sigma delta modulator BIST is presented. The modulator's static and dynamic parameters i.e. DNL, INL and SNR are obtained using CORDIC technique and are calculated using the proposed ORA circuit whose values are ± 0.2341, ± 0.2341 and 101.7833 respectively.

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